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09/586,961	06/05/2000	Akihiko Ohwada	1341.1048/JDH	8507

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/586,961	OHWADA, AKIHIKO	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the c ver sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 June 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 June 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-10 have been considered.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: IDS as received on 5 June 2000 and Priority Papers as received on 5 June 2000.

Drawings

3. Figure 27 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carnevale et al., U.S Patent Number 5,471,626 (herein referred to as Carnevale) in view of Applicant's admitted prior art (herein referred to as Prior Art).

8. Referring to claims 1-10, Carnevale has taught a pipeline operator comprising:

a. At least a first processing stage and a second processing stage (Applicant's claims 1, 2, 5, and 6) (Carnevale Abstract, lines 1-3; column 1, lines 32-40 and 64-67; Figure 3);

b. Latching units provided at input stage, between processing stages and at output stage of the first processing stage and the second processing stage respectively, which latching units hold processing data and processing results (Applicant's claims 1, 2, 5, and 6) (Carnevale column 3, lines 4-15);

c. First to n-th (n is a natural number such that $n > 1$) processing stages (Applicant's claim 3, 4, and 7-10) (Carnevale Abstract, lines 1-3; column 1, lines 32-40 and 64-67; Figure 3);

d. Latching units provided at input stage, between processing stages and at output stage of the first to n-th processing stages, which latching units hold processing data and processing results (Applicant's claim 3, 4, and 7-10) (Carnevale column 3, lines 4-15);

e. Wherein in decoding the instruction dispatched to the second processing unit, each instruction decoding unit decodes the instruction as the instruction to pass the processing data held in the latching unit on the upstream side through the first

processing unit (Applicant's claim 1) (Carnevale columns 1-2, lines 64-25; column 2, lines 31-44; Figure 3; and Figure 5);

f. Wherein in decoding the instruction dispatched to the first processing unit, each instruction decoding unit decodes the instruction as the instruction to pass the processing result of the first processing unit held in the latching unit on the upstream side through the second processing unit (Applicant's claim 2) (Carnevale columns 1-2, lines 64-25; column 2, lines 31-44; Figure 3; and Figure 5);

g. Wherein in decoding the instruction dispatched to an x-th (x is a natural number such that $x > 1$) processing unit, each instruction decoding unit decodes the instruction as the instruction to pass the processing data held in the latching unit on the upstream side through the first processing unit to the (x-1)-th processing unit (Applicant's claim 3) (Carnevale columns 1-2, lines 64-25; column 2, lines 31-44; Figure 3; and Figure 5).

h. Wherein in decoding the instruction dispatched to an x-th (x is a natural number such that $n > x$) processing unit, each instruction decoding unit decodes the instruction as the instruction to pass the processing result of the x-th processing unit held in the latching unit on the upstream side through the (x+1)-th processing unit to the n-th processing unit (Applicant's claim 4) (Carnevale columns 1-2, lines 64-25; column 2, lines 31-44; Figure 3; and Figure 5).

i. Wherein the instruction decoding units decode the instructions that have a correlation between the processing of the first processing unit and the processing

of the second processing unit that the processing result of the first processing unit becomes the processing data of the second processing unit, and further, in decoding the instruction to the second processing unit for executing the processing by itself, the instruction decoding unit decodes the instruction as the instruction to pass the processing data held in the latching unit on the upstream side through the first processing unit (Applicant's claim 5) (Carnevale columns 1-2, lines 64-25; column 2, lines 31-44; Figure 3; and Figure 5).

j. Wherein the instruction decoding units decode the instructions that have a correlation between the processing of the first processing unit and the processing of the second processing unit that the processing result of the first processing unit becomes the processing data of the second processing unit, and further, in decoding the instruction to the first processing unit for executing the processing by itself, the instruction decoding unit decodes the instruction as the instruction to pass the processing result of the first processing unit held in the latching unit on the upstream side through the second processing unit (Applicant's claim 6) (Carnevale columns 1-2, lines 64-25; column 2, lines 31-44; Figure 3; and Figure 5).

k. Wherein the instruction decoding units decode the instructions that have a correlation between m (m is a natural number such that $n > m$) stages of processing from an r-th (r is a natural number such that $r > 1$) processing unit to an s-th (s is a natural number such that $r < s < n$) processing unit out of the first processing unit to the n-th processing unit that the processing result of the pro-

stage processing unit becomes the processing data of the next-stage processing unit, and further, in decoding the instruction to an x-th (x is a natural number such that $r \leq x \leq s$) processing unit among the r-th processing unit to the s-th processing unit for executing the processing by the x-th processing unit by itself, the instruction 'decoding units decode the instructions as the instructions to pass the processing results held in the latching unit on the upstream side through the first processing unit to the (x-1)-th processing unit (Applicant's claim 7) (Carnevale columns 1-2, lines 64-25; column 2, lines 31-44; Figure 3; and Figure 5).

l. Wherein the instruction decoding units decode the instructions that have a correlation between m (m is a natural number-such that $n > m$) stages of processing from an r-th (r is a natural number such that $r > l$) processing unit to an s-th (s is a natural number such that $r < s < n$) processing unit out of the first processing unit to the n-th processing unit that the processing result of the pre-stage processing unit becomes the processing data of the next-stage processing unit, and further, in decoding the instructions to an x-th (x is a natural number such that $r \leq x \leq s$) processing unit to an (x+p)-th (p is a natural number such that $p < s-r$) processing unit among the r-th processing unit to the s-th processing unit for completing the execution of one processing by the processing units of p stages, the instruction decoding units decode the instructions as the instructions to pass the processing data held in the latching unit on the upstream side through the first processing unit to the (x-1)-th processing unit (Applicant's claim 8)

(Carnevale columns 1-2, lines 64-25; column 2, lines 31-44; Figure 3; and Figure 5).

m. Wherein the instruction decoding units decode the instructions that have a correlation between m (m is a natural number such that $n > m$) stages of processing from an r-th (r is a natural number such that $r > 1$) processing unit to an s-th (s is a natural number such that $r < s < n$) processing unit out of the first processing unit to the n-th processing unit that the processing result of the pre-stage processing unit becomes the processing data of the next-stage processing unit, and further, in decoding the instruction to an x-th processing unit (x is a natural number such that $r \leq x \leq s$) among the r-th processing unit to the s-th processing unit for the x-th processing unit to execute the processing by itself, the instruction decoding units decode the instructions as the instructions to pass the processing result of the x-th processing unit held in the latching unit on the upstream side through the (x+1)-th processing unit to the n-th processing unit (Applicant's claim 9) (Carnevale columns 1-2, lines 64-25; column 2, lines 31-44; Figure 3; and Figure 5).

n. Wherein the instruction decoding units decode the instructions that have a correlation between m (m is a natural number such that $n > m$) stages of processing from an r-th (r is a natural number such that $r > 1$) processing unit to an s-th (s is a natural number such that $r < s < n$) processing unit out of the first processing unit to the n-th processing unit that the processing result of the pre-stage processing unit becomes the processing data of the next-stage processing

unit, and further, in decoding the instructions to an (x-p)-th processing unit to an x-th (x and p are natural numbers such that $r \leq x \leq s$ and $p \leq s-r$) processing unit among the r-th processing unit to the s-th processing unit for completing the execution' of one processing by the processing units of p stages, the instruction decoding units decode the instructions as the instructions to pass the processing results of the (x-p)-th processing unit to the x-th processing unit held in the latching unit on the upstream side through the (x+l)-th processing unit to the n-th processing unit (Applicant's claim 10) (Carnevale columns 1-2, lines 64-25; column 2, lines 31-44; Figure 3; and Figure 5).

9. Carnevale has not explicitly taught:

a. A first processing unit provided at the first processing stage, which first processing unit carries out a processing according to an instruction by using the processing data held in the latching unit on the upstream side and for outputting the processing result to the latching unit on the downstream side (Applicant's claims 1, 2, 5, and 6);

b. A second processing unit provided at the second processing stage, which second processing unit carries out a processing according to an instruction by using the processing data held in the latching unit on the upstream side and for outputting a processing result to the latching unit on the downstream side (Applicant's claims 1, 2, 5, and 6);

c. Instruction decoding units for decoding the instructions dispatched to the first processing unit and the second processing unit respectively (Applicant's claims 1, 2, 5, and 6);

d. First to n-th processing units provided at the first to n-th processing stages respectively, which processing unit carries out a processing according to an instruction by using the processing data held in the latching unit on the upstream side and for outputting the processing result to the latching unit on the downstream side (Applicant's claim 3, 4, and 7-10); and

e. Instruction decoding units for decoding the instructions dispatched to the first to n-th processing units respectively (Applicant's claim 3, 4, and 7-10).

10. However, Carnevale has taught each pipeline stage executes particular operations related to a certain purpose and control words, similar to instructions, which control the exact operations completed during each stage. Prior Art has explicitly taught:

a. A first processing unit provided at the first processing stage, which first processing unit carries out a processing according to an instruction by using the processing data held in the latching unit on the upstream side and for outputting the processing result to the latching unit on the downstream side (Applicant's claims 1, 2, 5, and 6) (Applicant's claims 1 and 2) (Prior Art page 2, lines 1-6; page 3, lines 21-23; and Figure 27);

b. A second processing unit provided at the second processing stage, which second processing unit carries out a processing according to an instruction by using the processing data held in the latching unit on the upstream side and for outputting a

processing result to the latching unit on the downstream side (Applicant's claims 1, 2, 5, and 6) (Prior Art page 2, lines 1-6; page 4, lines 9-13; and Figure 27);

c. Instruction decoding units for decoding the instructions dispatched to the first processing unit and the second processing unit respectively (Applicant's claims 1, 2, 5, and 6) (Prior Art page 3, lines 15-21; page 4, lines 7-9; and Figure 27);

d. First to n-th processing units provided at the first to n-th processing stages respectively, which processing unit carries out a processing according to an instruction by using the processing data held in the latching unit on the upstream side and for outputting the processing result to the latching unit on the downstream side (Applicant's claim 3, 4, and 7-10) (Prior Art page 2, lines 1-6; page 3, lines 21-23; and Figure 27); and

e. Instruction decoding units for decoding the instructions dispatched to the first to n-th processing units respectively (Applicant's claim 3, 4, and 7-10) (Prior Art page 3, lines 15-21; page 4, lines 7-9; and Figure 27).

11. Since each stage performs certain operations on data in order to produce output reflecting the purpose of the stage, there must be some way to determine and control which operations are performed on the data and something to actually perform the operations of each stage. It would have been obvious to a person of ordinary skill in the art to incorporate the processing units and decoder of Prior Art in the device of Carnevale, because they are necessary for the stages of Carnevale to determine which operations to perform on the data and to actually perform the operations. Therefore, it would have been obvious to a person of ordinary skill in the art at the

time this invention was made to incorporate the processing units and decoder of Prior Art in the device of Carnevale.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Kanuma, U.S. Patent Number 5,165,034, has taught a system with multiple operational units and a bypass to send data to the units.

b. Nugent, U.S. Patent Number 5,333,284, has taught a pipelined processor with operational units at each stage, and latches before the operational units.

c. Glew, U.S. Patent Number 5,619,664, has taught a multiple staged pipelined processor with data forwarding.

d. Heikes et al., U.S. Patent Number 5,740,181, has taught a multiple staged pipeline with latches before the stages.

e. Petolino, Jr., U.S. Patent Number 5,918,034, has taught a multiple staged pipeline with latches and stage bypass.

f. Makineni et al., U.S. Patent Number 5,996,065, has taught a multiple clock cycle pipeline with bypass control.

g. Blomgren et al., U.S. Patent Number 6,460,134, has taught a pipeline of functional units with latches between the functional units.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

14. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

15. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Aimee J. Li
Examiner
Art Unit 2183

May 2, 2003

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100